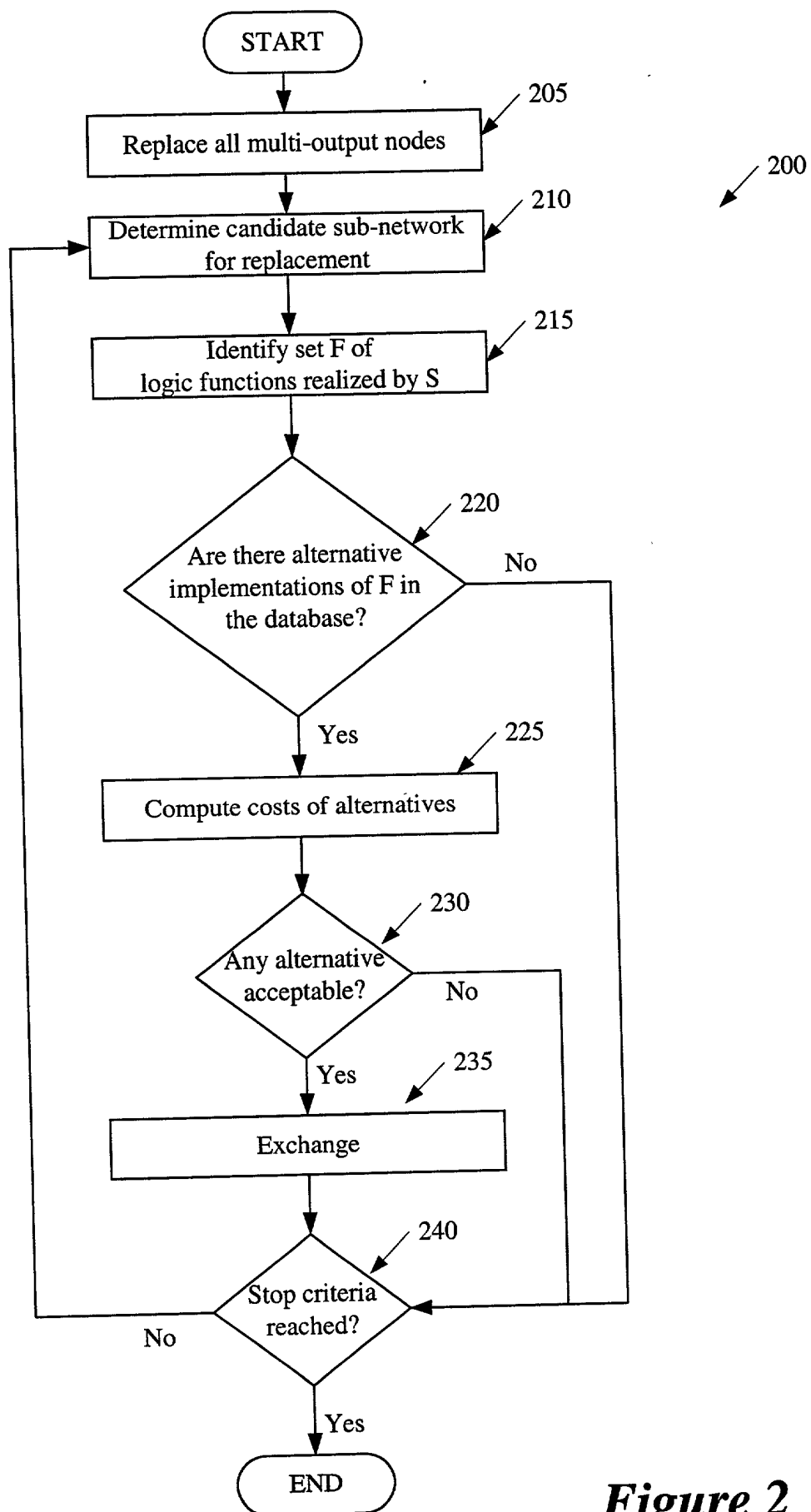
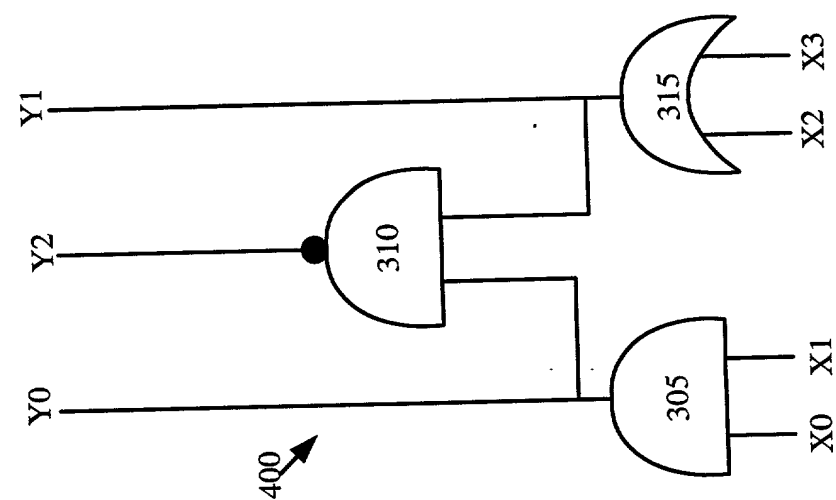


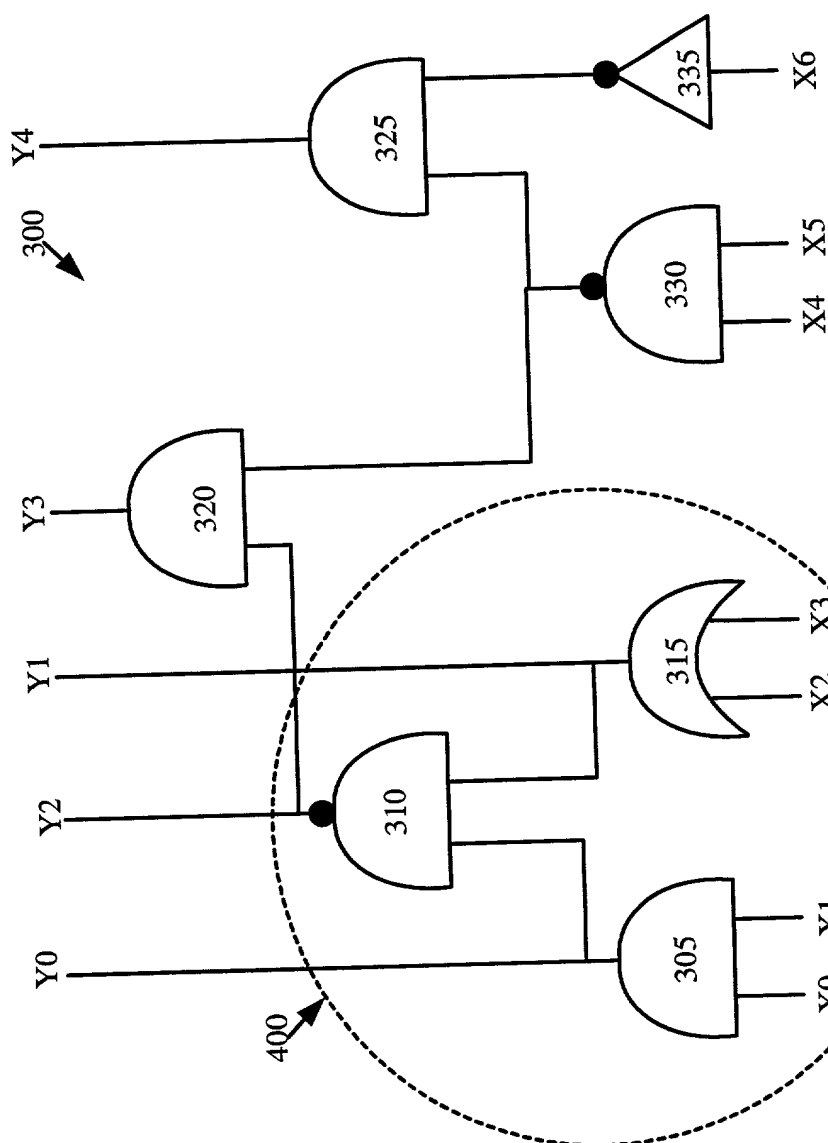
*Figure 1*



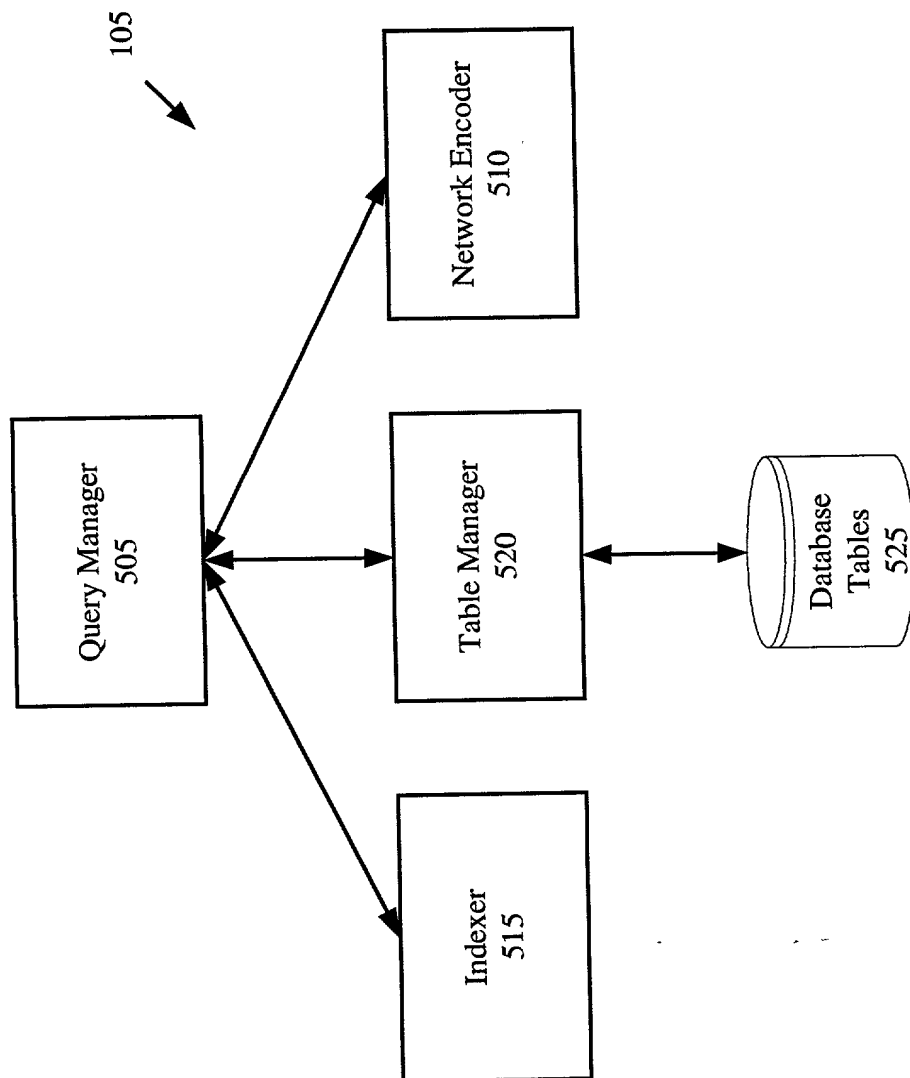
**Figure 2**



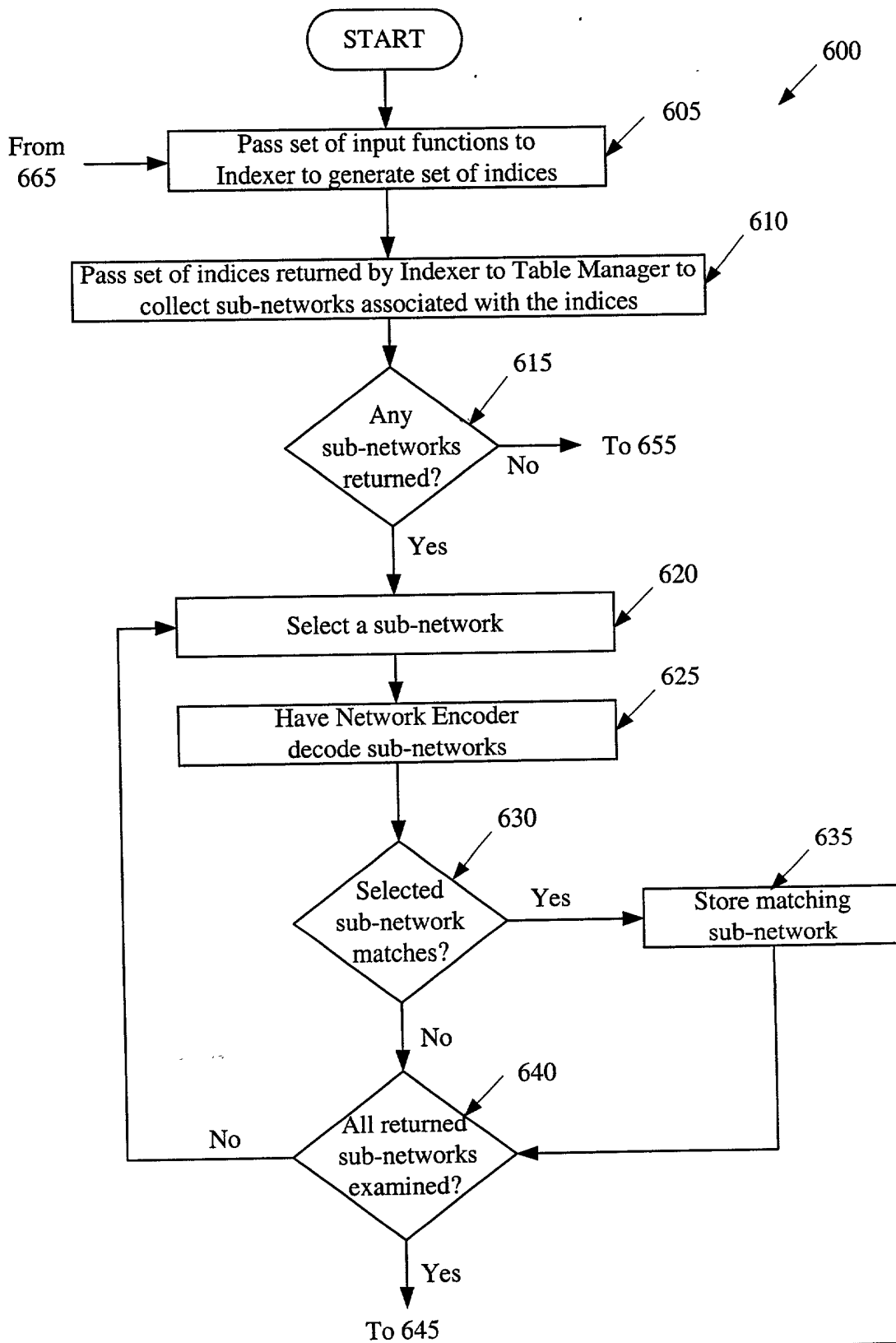
**Figure 4**



**Figure 3**

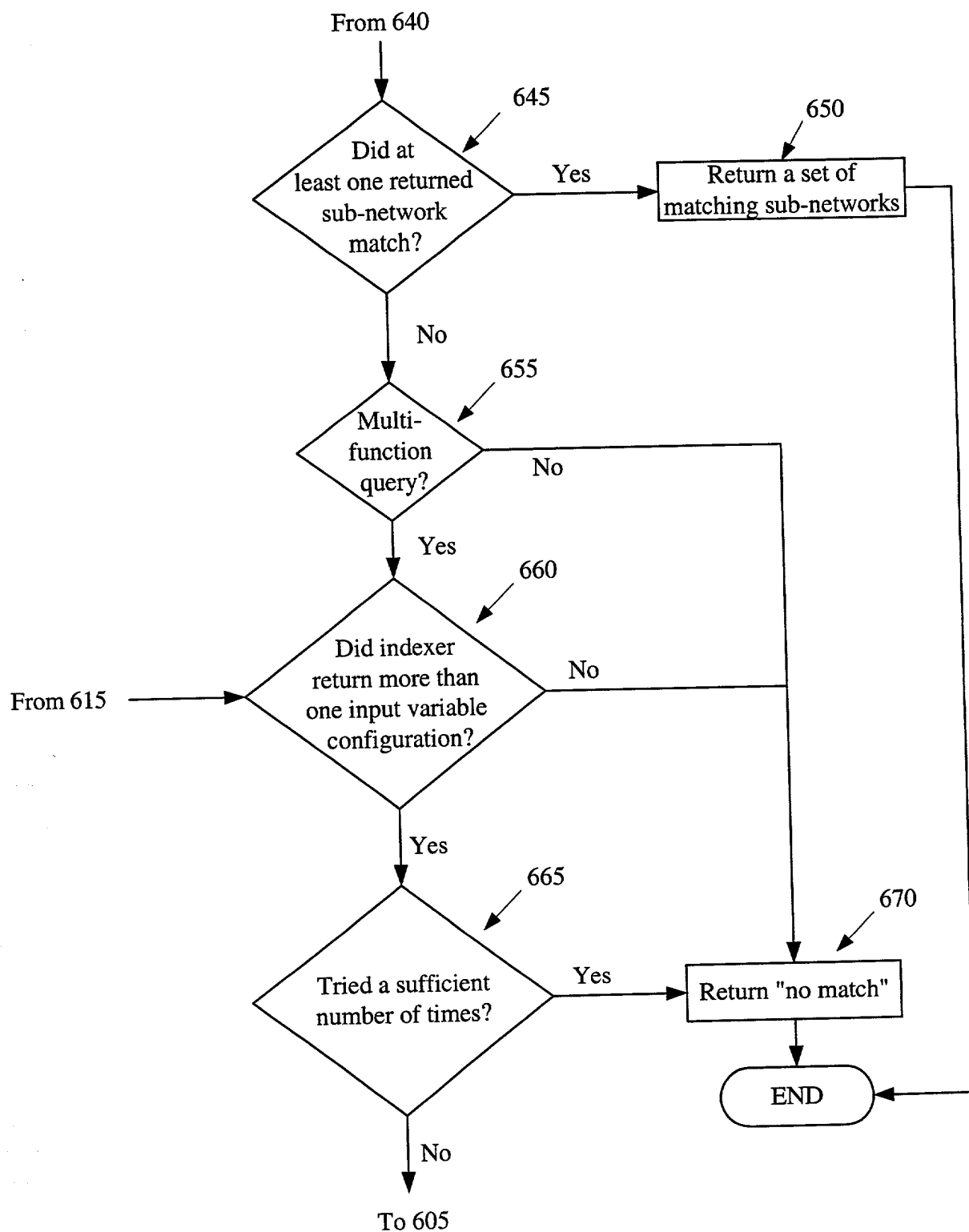


**Figure 5**

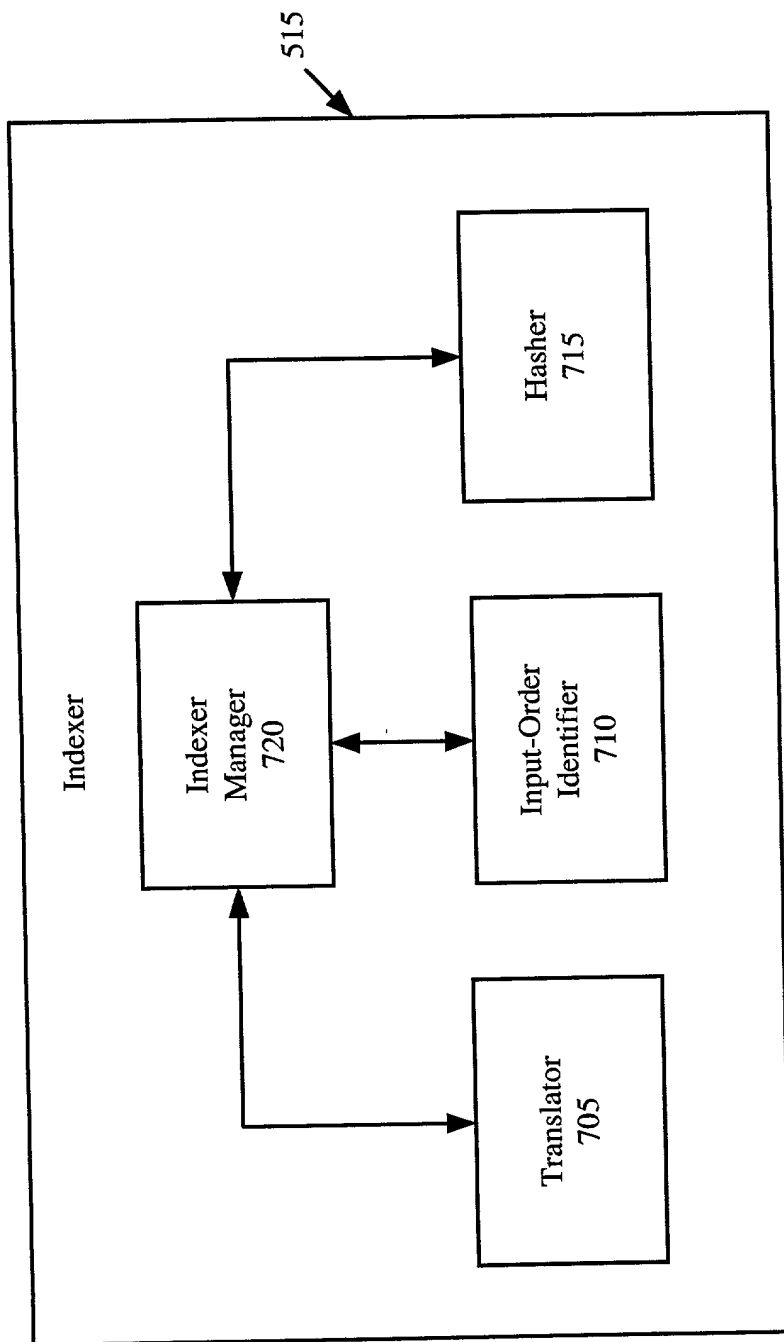


**Figure 6A**

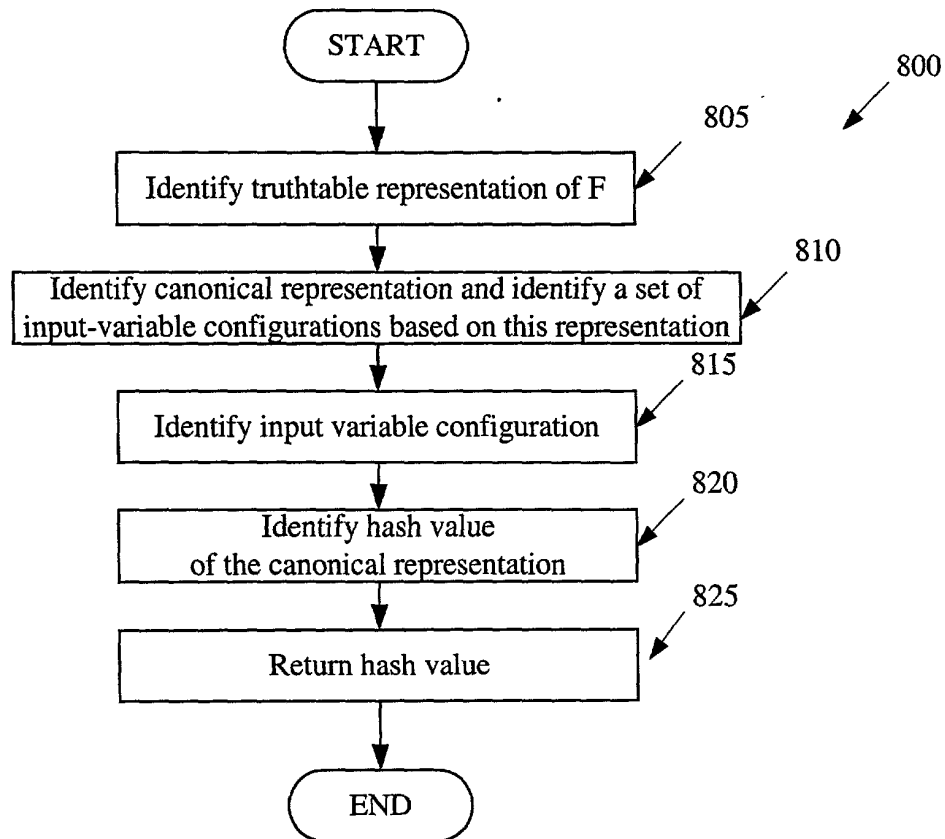
**Figure 6:** Figure 6A  
Figure 6B



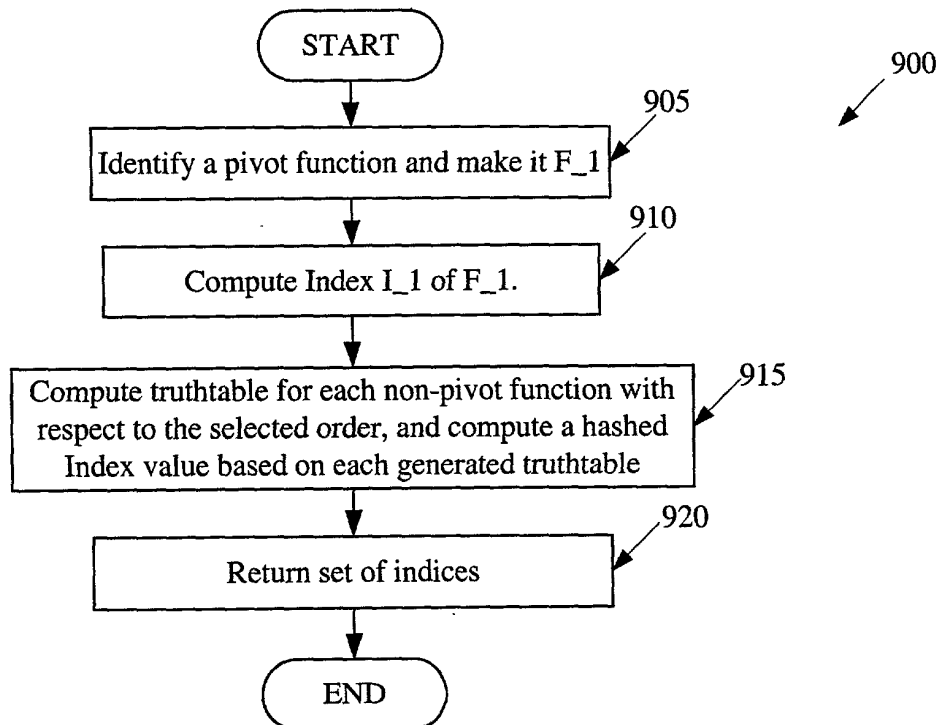
**Figure 6B**



*Figure 7*



**Figure 8**

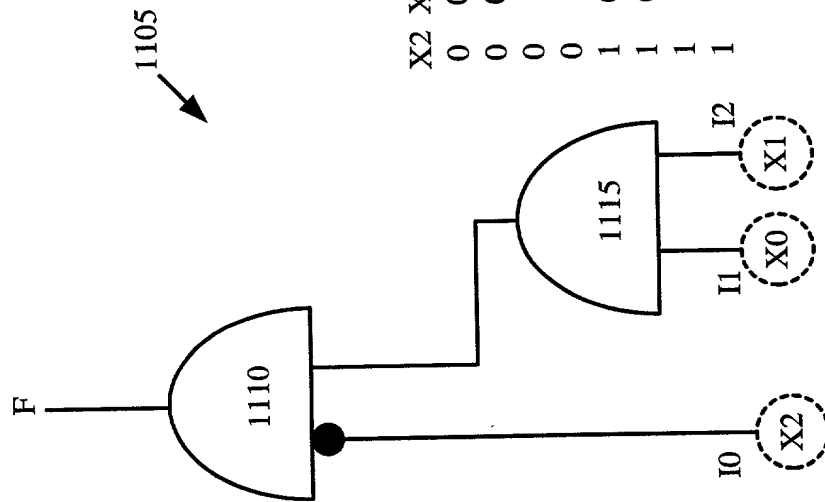


**Figure 9**



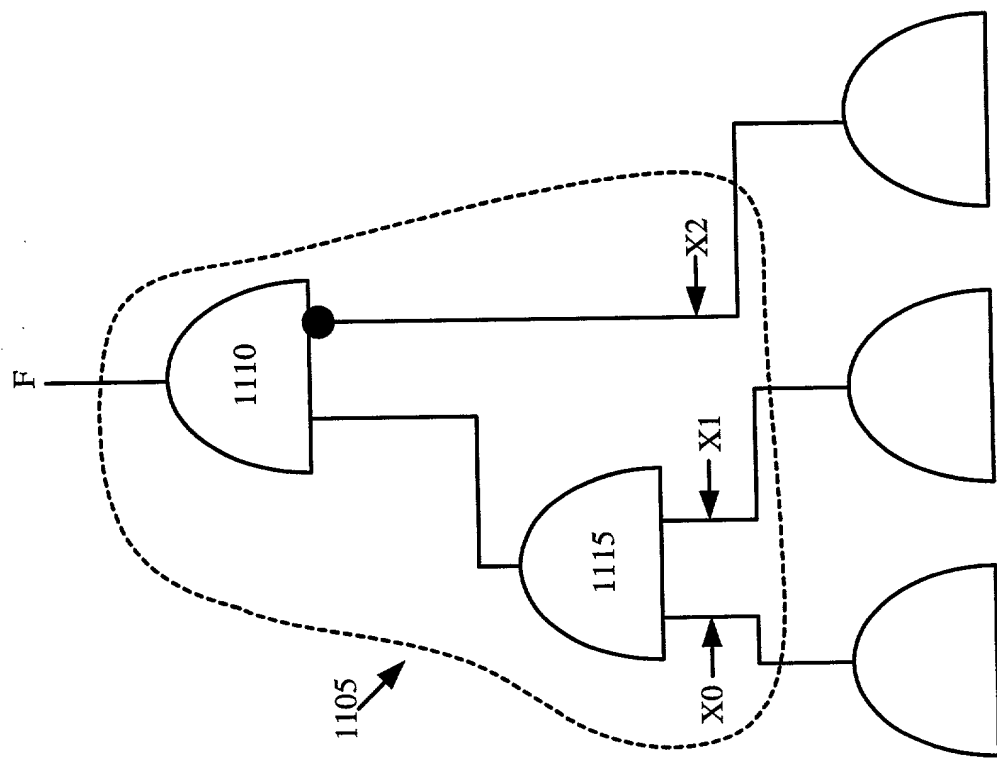


FIG. 12 is a schematic diagram of a logic circuit 1105. The circuit includes an AND gate 1110 with inputs F and I0 (labeled X2). The output of gate 1110 is connected to an AND gate 1115. Gate 1115 has inputs I1 (labeled X0) and I2 (labeled X1). The output of gate 1115 is connected to a third AND gate. The inputs to this third gate are the output of gate 1115 and the output of gate 1110. The output of the third gate is labeled F. A dashed line 1105 encloses the entire circuit.



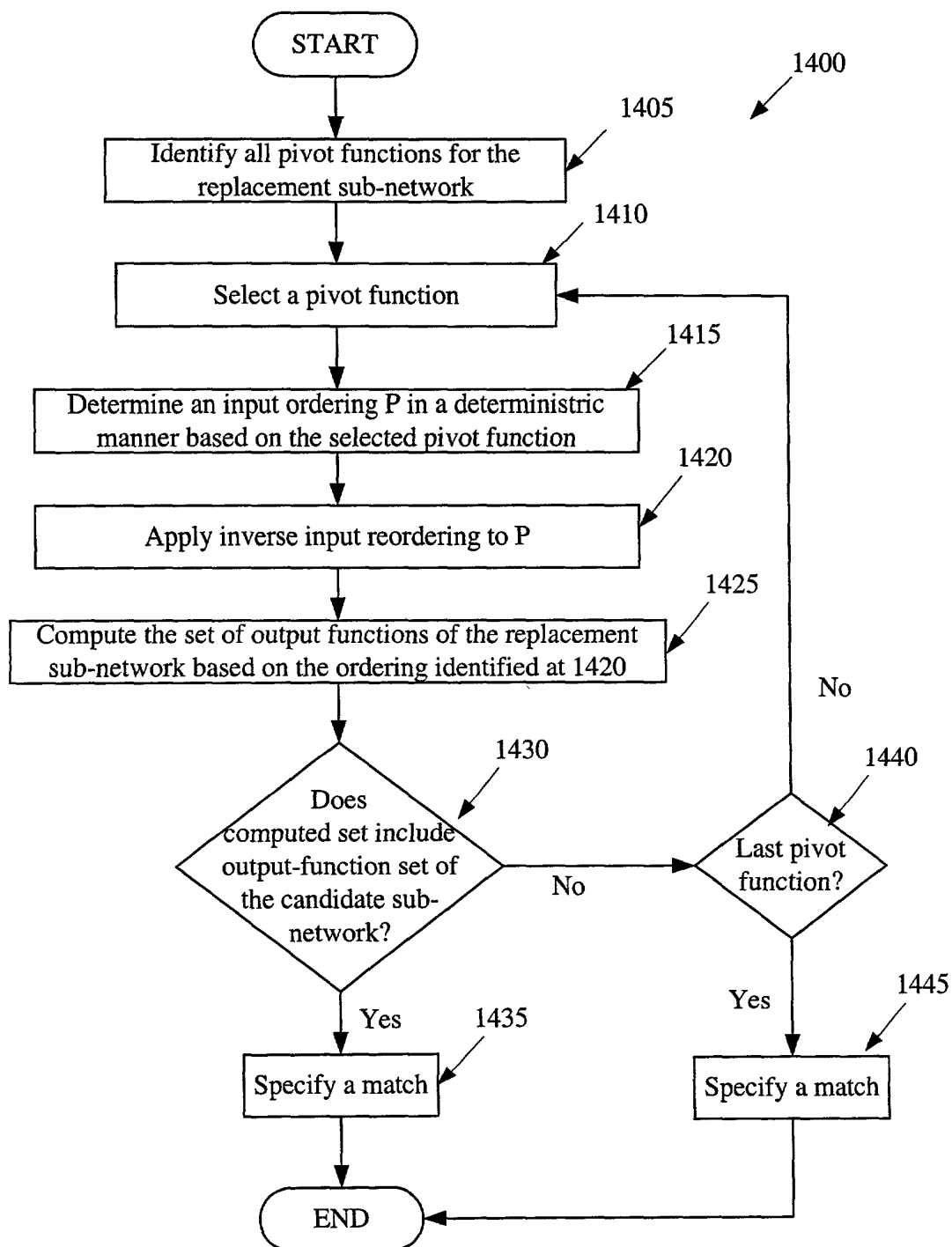
X2	X1	X0	TT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Figure 12



X2	X1	X0	TT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Figure 13



**Figure 14**

FIG. 15 is a schematic diagram of a network structure 1500. The network structure 1500 includes a set of nodes 1505 and a set of links 1510. The nodes 1505 are arranged in a grid-like pattern, and the links 1510 connect the nodes 1505. The network structure 1500 is used to illustrate a network topology.

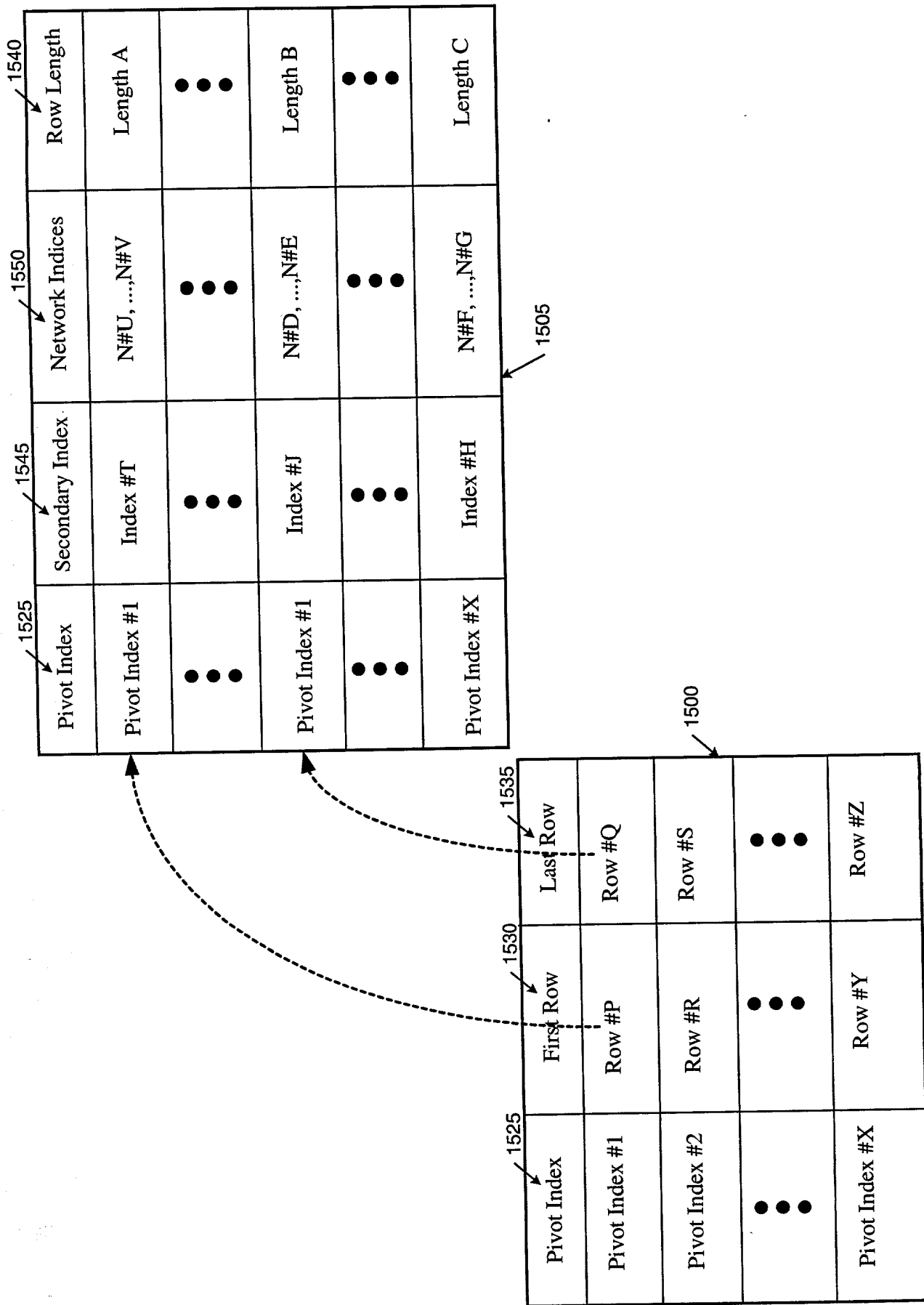


Figure 15

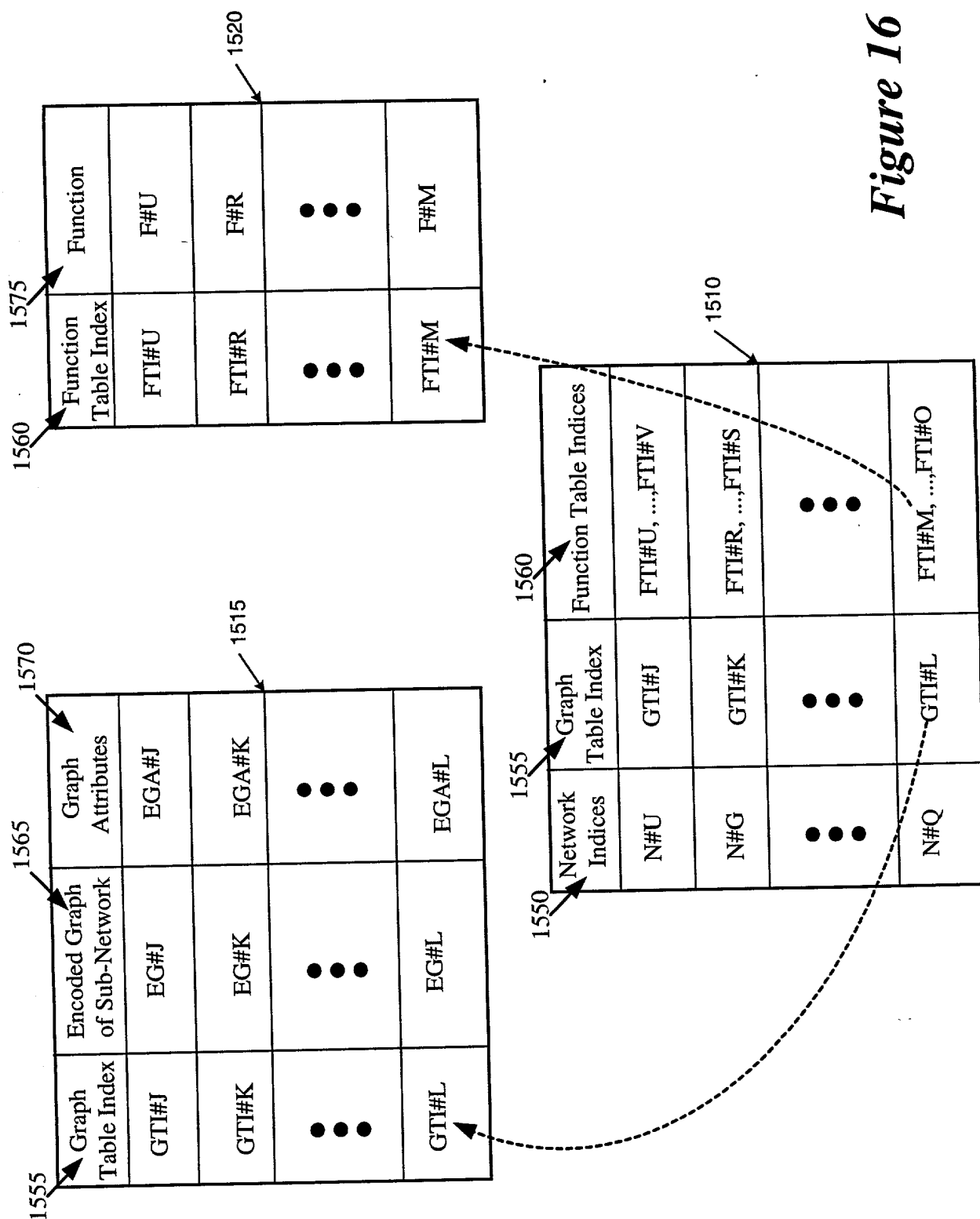
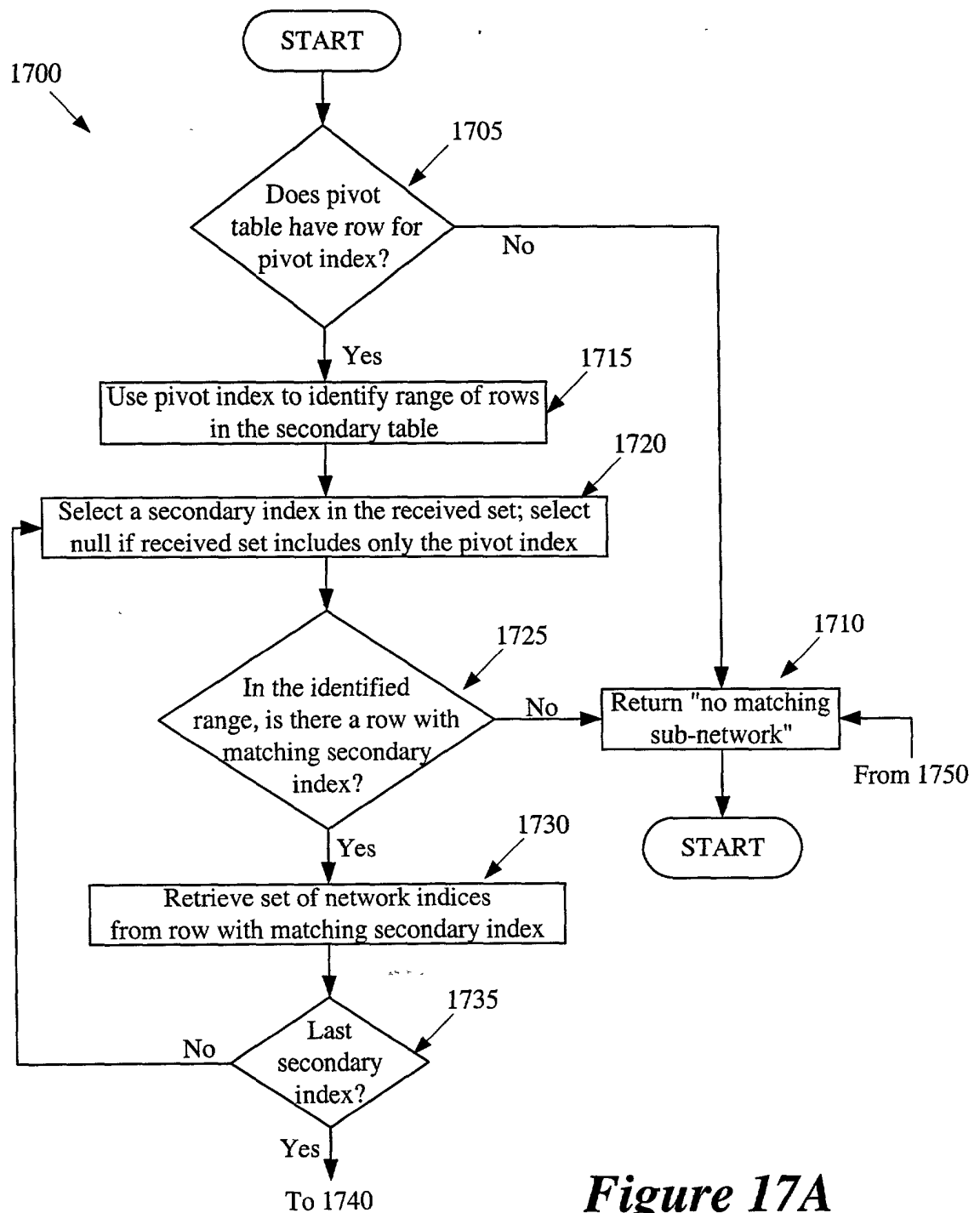
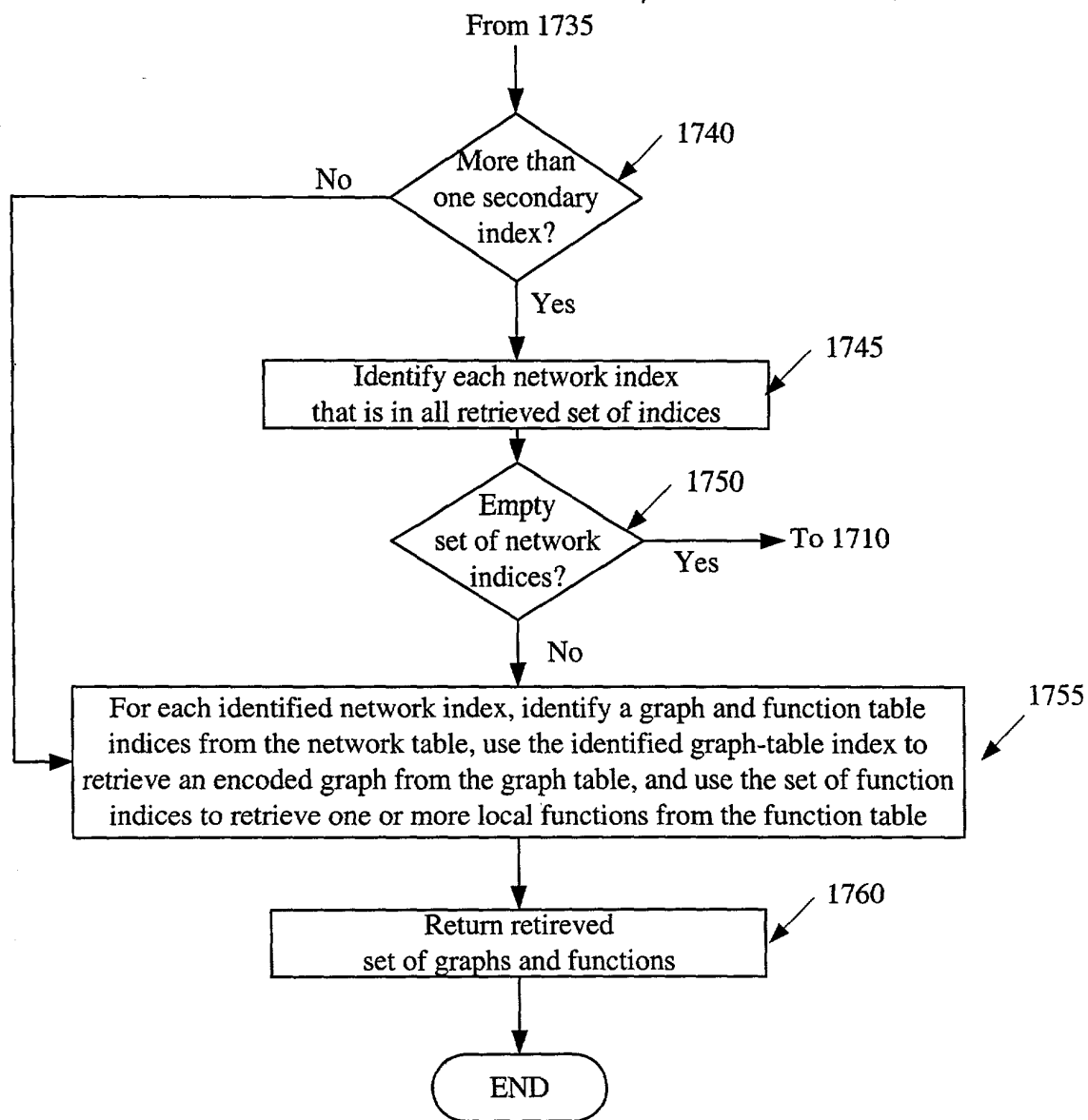


Figure 16

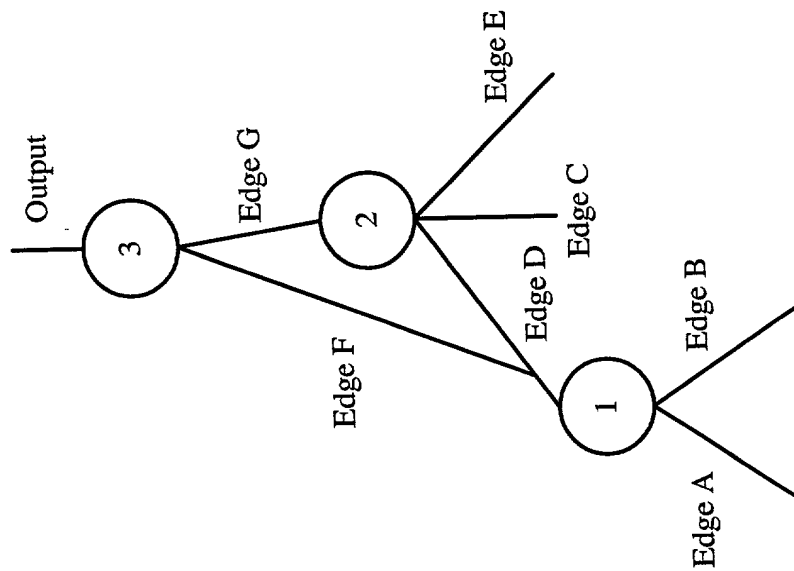


**Figure 17A**

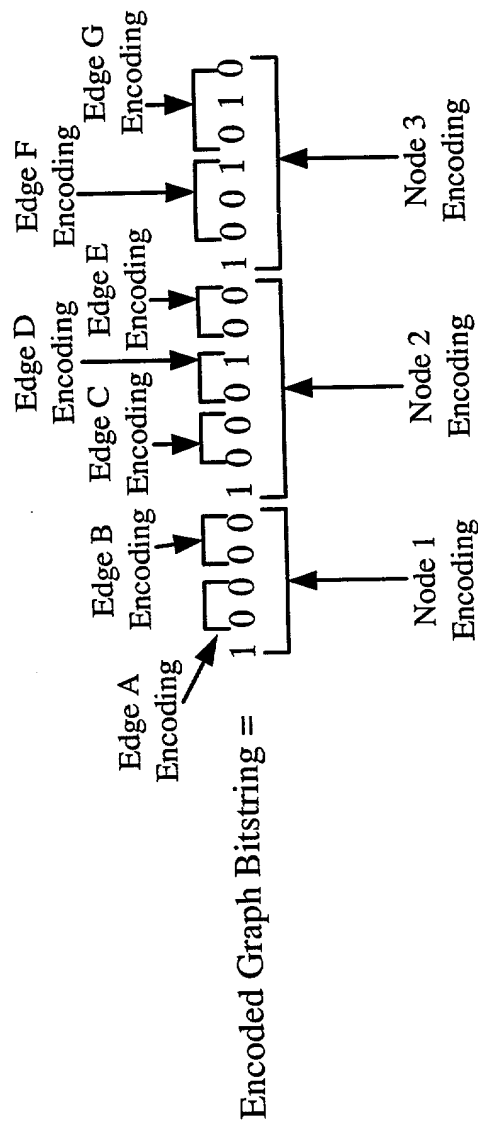
**Figure 17:** Figure 17A  
Figure 17B



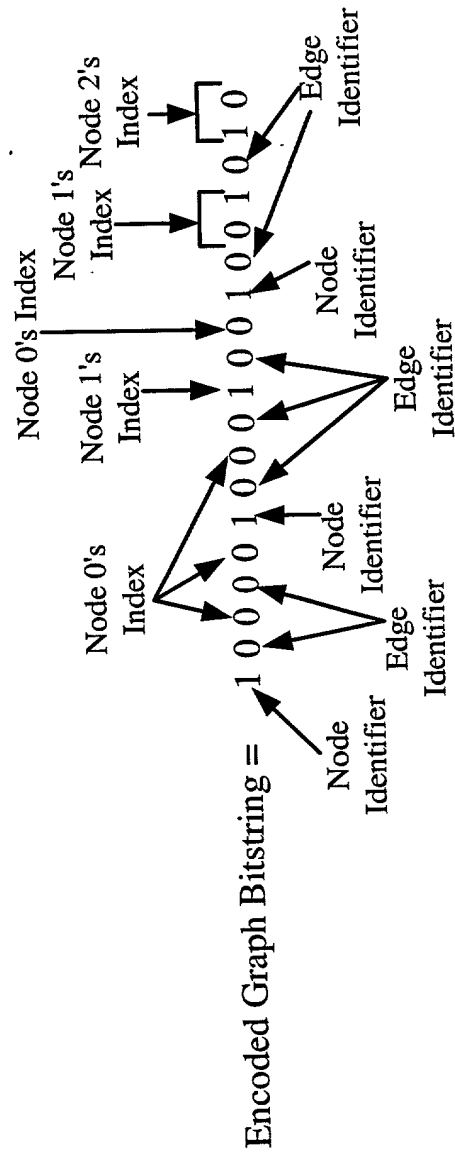
**Figure 17B**



**Figure 18**

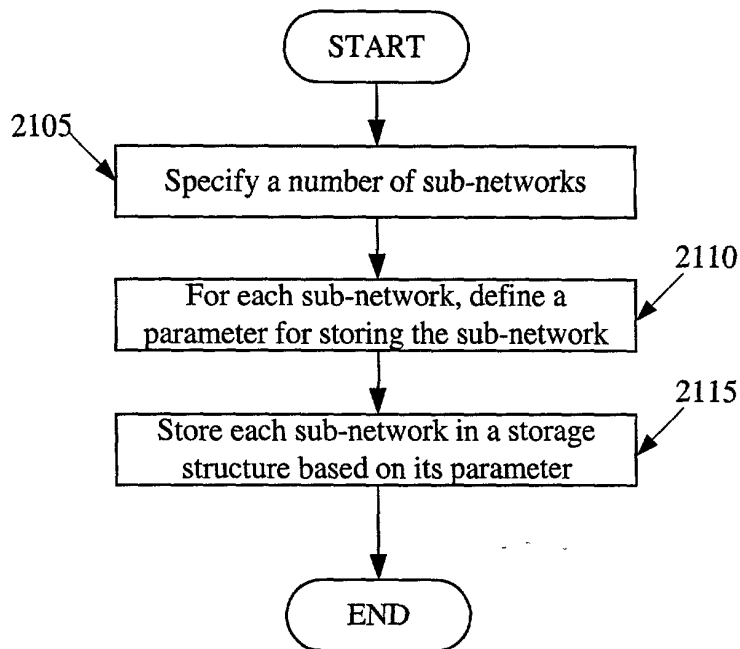


**Figure 19**

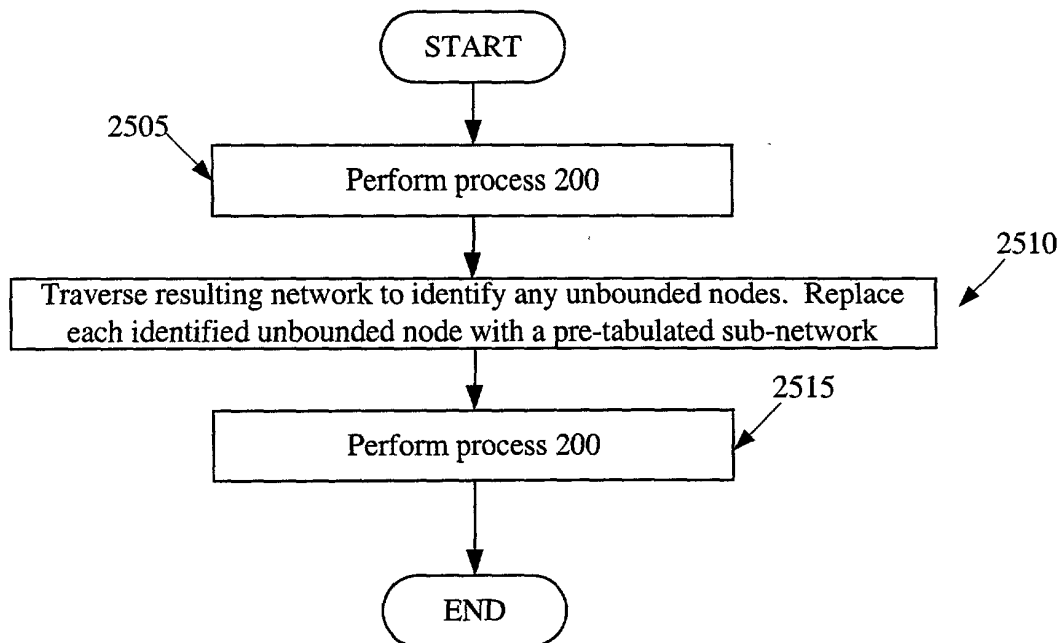


**Figure 20**

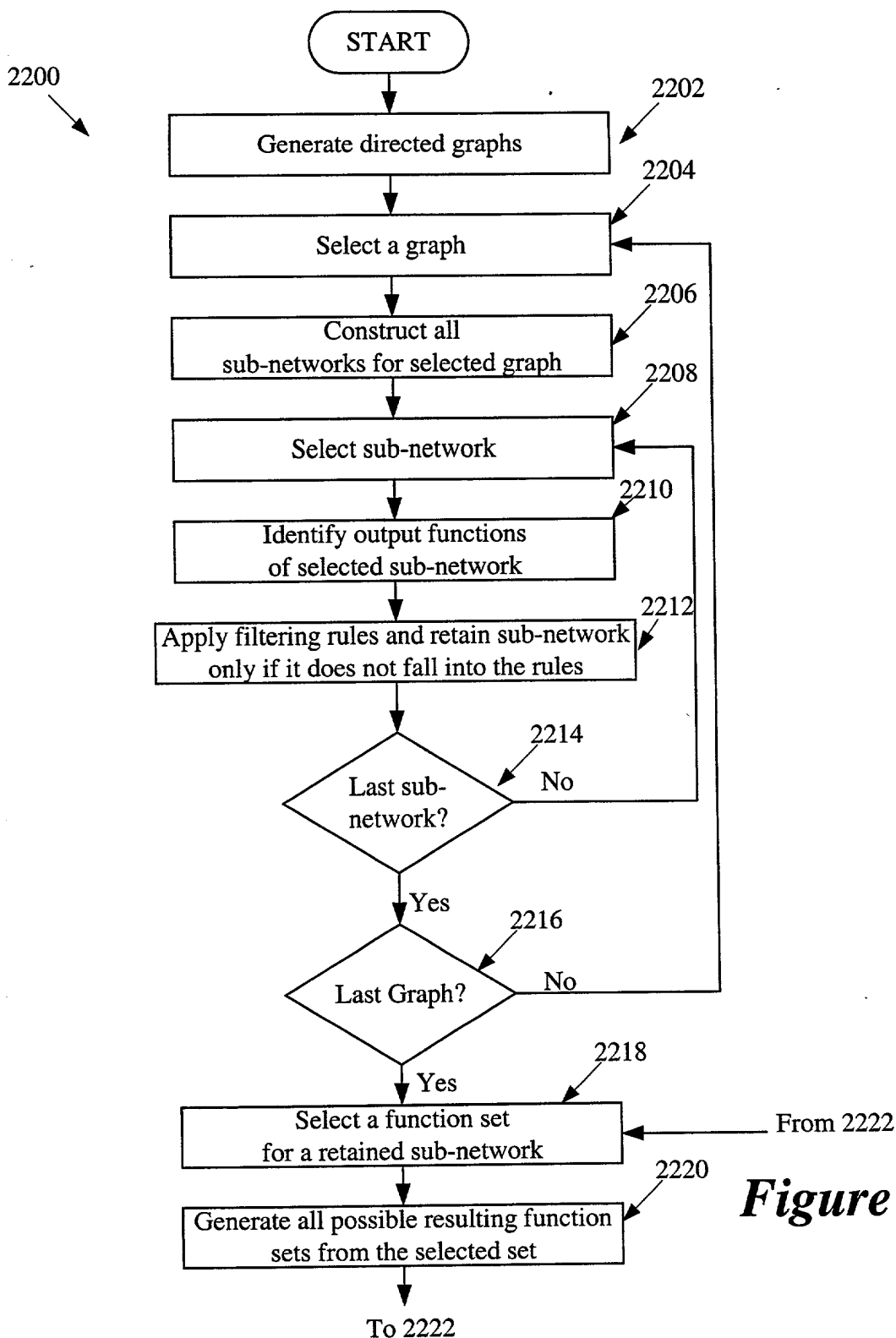




**Figure 21**

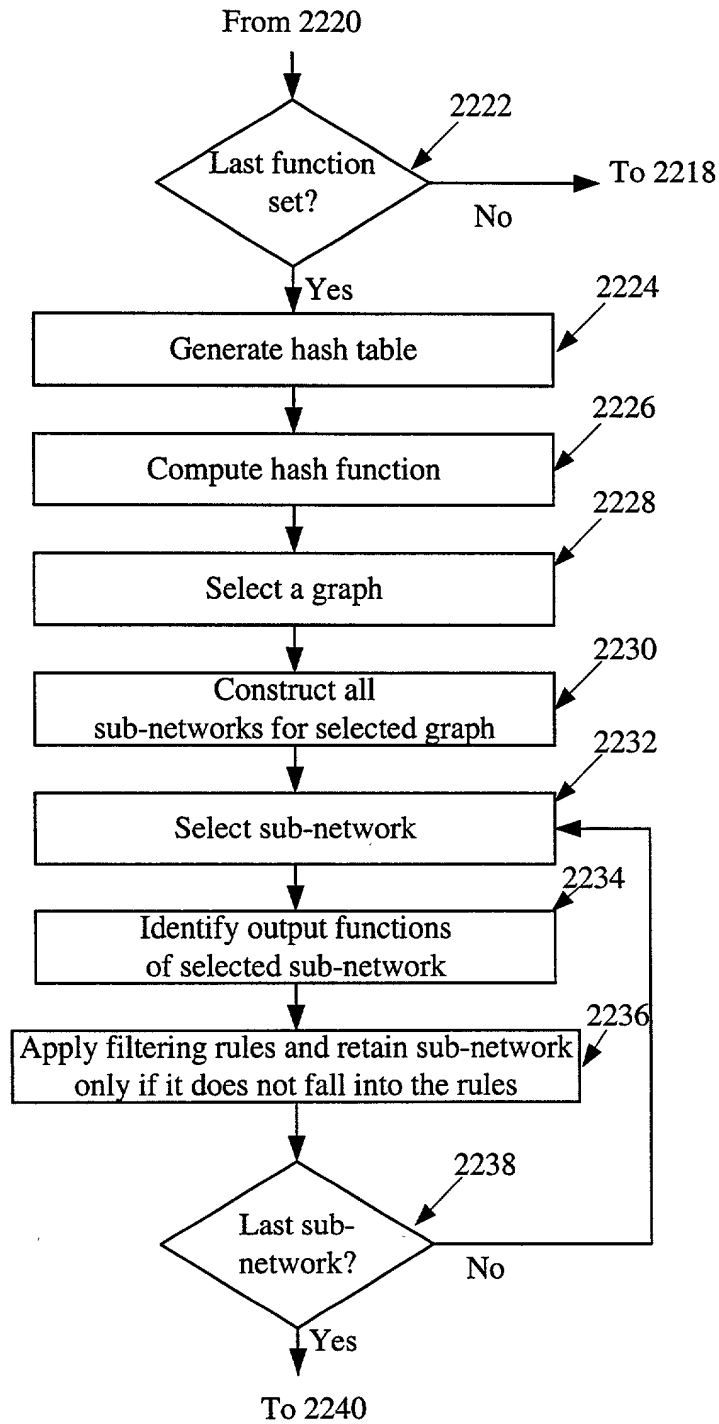


**Figure 25**

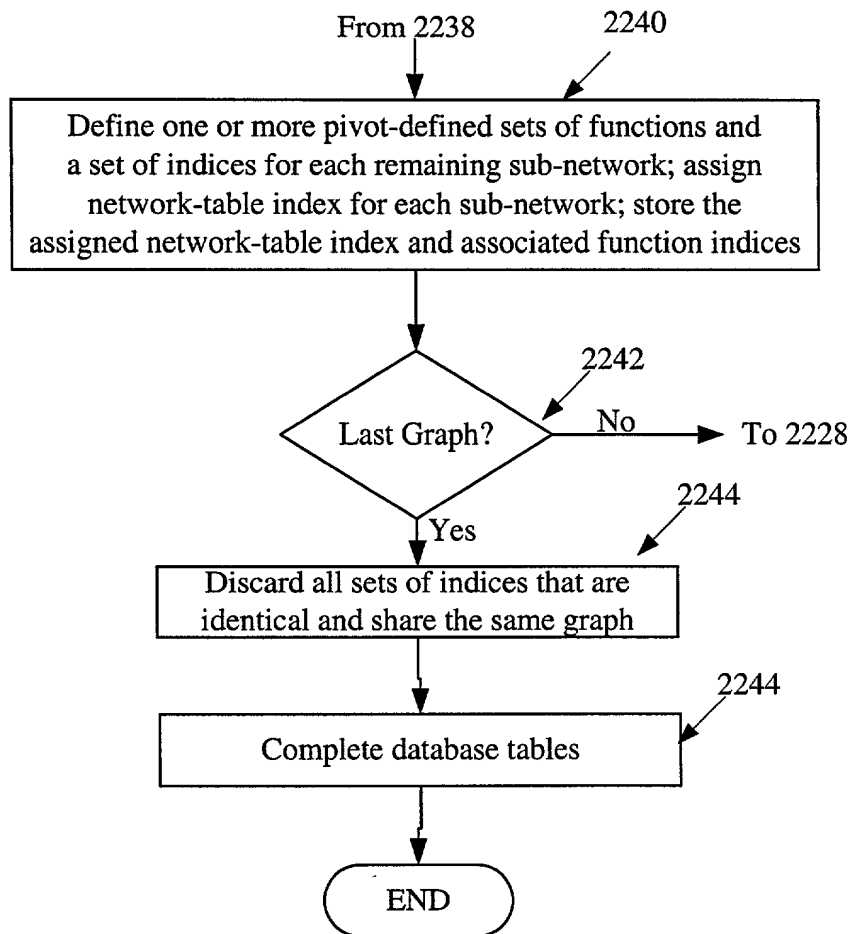


**Figure 22A**

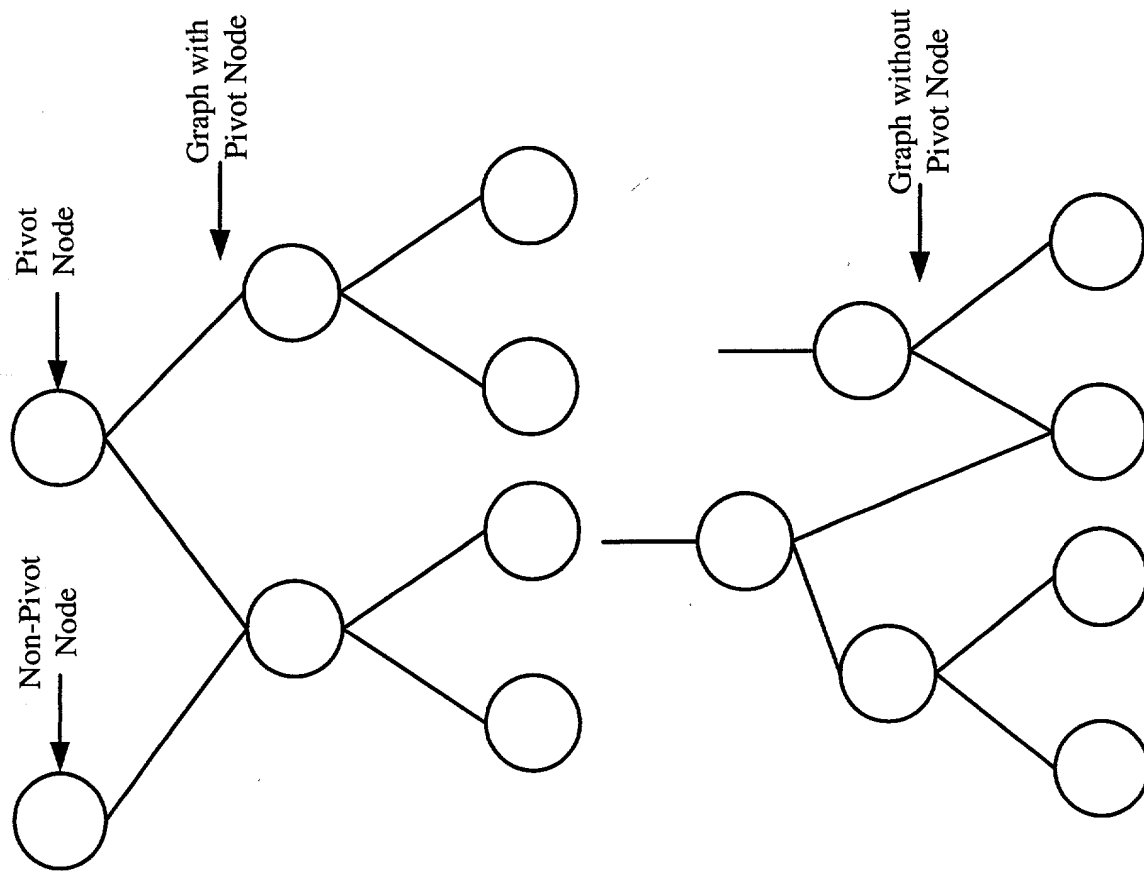
**Figure 22:** Figure 22A  
Figure 22B  
Figure 22C



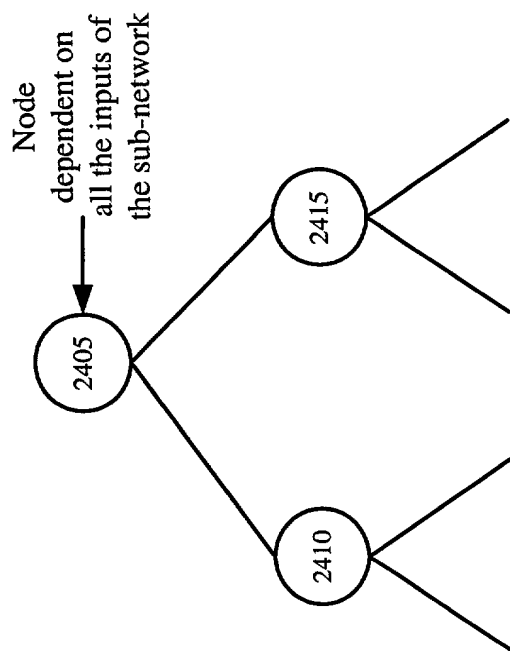
**Figure 22B**



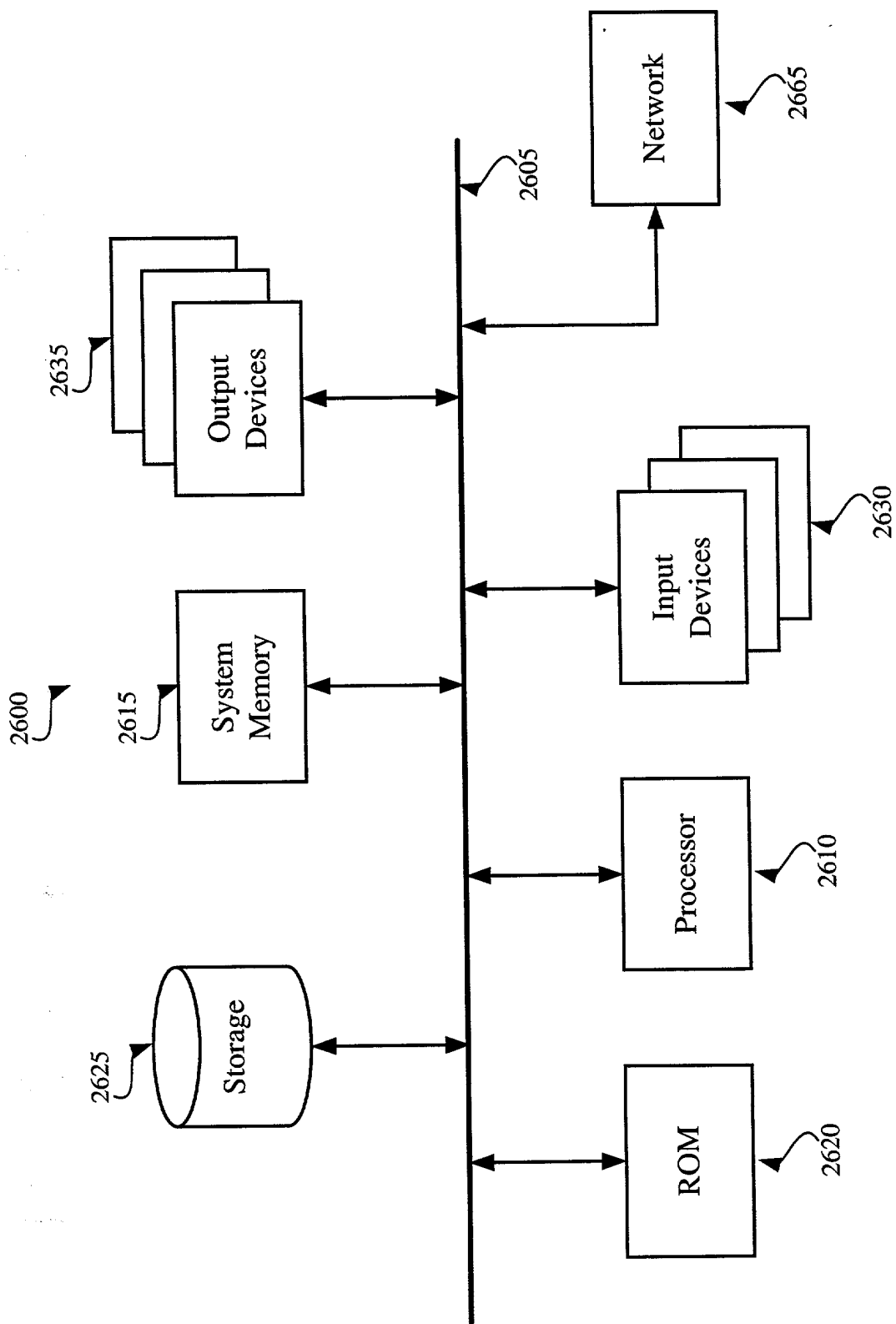
**Figure 22C**



**Figure 23**



**Figure 24**



*Figure 26*